AM5K2Ex KeyStone Multicore ARM® System-on-Chips

Overview

The AM5K2Ex platform is derived from TI's industry-proven KeyStone II architecture and is TI's first infrastructure-grade embedded multicore ARM device. The AM5K2Ex SoC combines excellent single-threaded performance from a quad ARM Cortex™-A15 MPCore™ processor with 4MB of layer 2 cache. Packet and security coprocessors as well as layer 2 Ethernet switching and integrated infrastructure interfaces like 1Gb/10Gb Ethernet, PCIe and USB3 enable a wide variety of high-performance applications. The AM5E2Ex SoC provides 19600 DMIPS of compute performance with TI's industry-leading external memory controller technology – multicore shared memory controller (MSMC). Due to its optimized performance profile, AM5K2Ex SoC is ideally suited for applications like cloud infrastructure, networking control plane, routers, switches, wireless transport, wireless core network and industrial sensor networks. TI also provides extensive software support in collaboration with commercial providers to enable rapid time to market with the AM5K2Ex SoC.

Power and Performance

The AM5K2Ex platform provides 5.6 GHz of Cortex-A15 processor performance resulting in 19200 DMIPS that is integrated with TI's best-in-class interconnect results in the best single-threaded performance for an infrastructure SoC. These SoCs deliver new levels of power savings, achieving a power consumption of as little as 6 Watts on the AM5K2E02 SoC.

Fast and Wide Packet Interfaces

Processing performance alone does not differentiate infrastructure from consumer

Key Features

Key features of AM5K2Ex devices include:

CorePac Processors

- Up to four ARM Cortex™-A15 MPCore™ processors, 19600 Dhrystone MIPS

Network AcceleratorPac

- Packet coprocessor (IPv4/IPv6) for Layer 2–4
- Security coprocessor IPSec/SRTP
- Five-port 1Gb Ethernet switch
- Three-port 10Gb Ethernet switch

Memory

- Cache-coherent Multicore Shared Memory Controller (MSMC)
- 1MB per core Level 2 RAM/cache
- 2MB shared memory with ECC and cache coherency
- One DDR3/3L 1600 interfaces with ECC

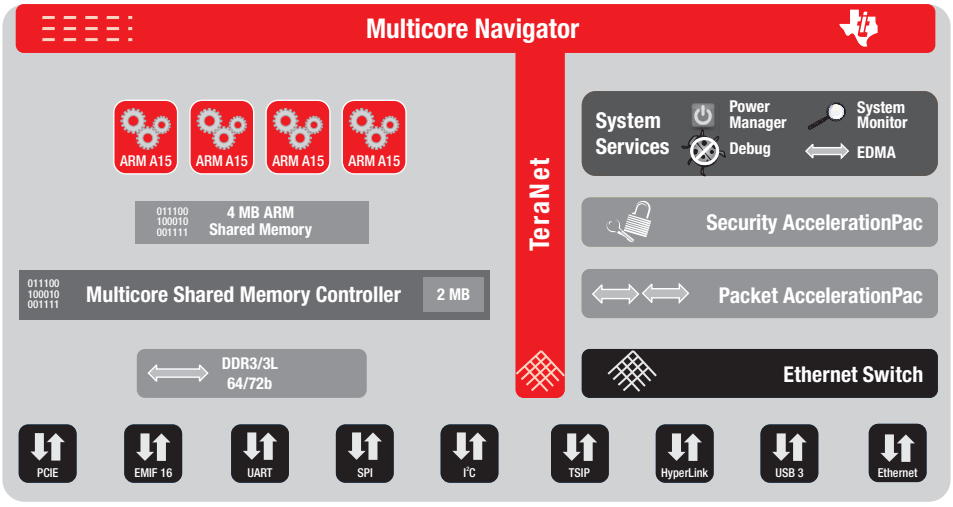
KeyStone II Architecture

- Multicore Navigator; brings single-core programming simplicity to multicore SoCs
- 8,000 atomic hardware queues
- TeraNet – on-chip interconnect providing more than 2 terabits per second throughput
- Low power – 6–8 Watts at 55°C case temperature, 6 Watts typical for AM5K2E02 SoC

High speed I/O

- PCI Express Gen2—up to 10 Gbps
- USB 3.0
- 10Gb Ethernet
- HyperLink – up to 50 Gbaud for chip-to-chip interconnect

For more technical detail see the **data sheet**.



TI's KeyStone AM5K2E04 SoC

applications. High-performance networking interfaces are critical to deliver data to processors fast enough. The addition of an on-chip five-port 1Gb Ethernet switch, three-port 10Gb Ethernet switch, packet coprocessor and security coprocessor provides carrier-grade Ethernet throughput without the increase in ARM® processor loading that normally comes from layer 2–4 processing, encryption and decryption. Other high-performance SerDes interfaces like PCIe, deliver data to processors at infrastructure speeds, enabling the AM5K2Ex platform to handle tremendous data throughput.

The TeraNet is a multilevel interconnection of high-speed non-blocking channels that delivers more than two terabits per second of concurrent throughput – enabling full multicore entitlement in which every processing element can operate near full capacity all of the time.

The 50-Gbaud HyperLink uses a low-overhead protocol that extends the TeraNet off the device to other KeyStone SoCs and third-party devices, making them appear as one larger device while simplifying software development, reducing latency and improving system performance.

High-Speed Memory for Demanding Applications

Infrastructure applications demand non-blocking, high-performance memory with error correction. For KeyStone II, TI upgraded the multicore shared memory controller (MSMC) so that memories can operate at the speed of the processor cores, which reduces latency and contention while providing high-bandwidth interconnections between processor cores and shared internal and external memory. The 72-bit DDR3/3L controllers run at 1600 MT/s with optional error correction (ECC) support and hardware-based cache coherency, enabling more than 12.8-Gbps data transfers between external and internal memory.

Tools and Software to Reduce Development Time

Texas Instruments' development tools and runtime software support make migration and development for the multicore ARM platform simpler than ever.

The Multicore Software Development Kit (MCSDK) provides support for open source Linux™ and TI's SYS/BIOS™ operating system for ARM cores. Evaluation modules (EVMs) will be available with the MCSDK and preloaded example projects.

TI is a founding member for Yocto along with Linux Foundation and has been working on defining commonly accepted embedded Linux distribution standards. TI's MCSDK will provide Yocto-compliant Linux distribution leveraging and enabling latest OS version as well as open-source software packages. Customers also have an option to work with commercial software providers to get commercially supported OS or software packages.

Code Composer Studio™ Integrated Development Environment (IDE) provides a development environment that reduces porting time and can be used as a plug-in to the open-source Eclipse Integrated Development Environment. TI also plans to support open-source development and profiling tools for KeyStone-II-based SoCs. Support for other real-time OS will be available in near future.

For more information about the AM5K2Ex platform and TI's portfolio of KeyStone multicore devices please visit **www.ti.com/multicore**.